

REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Disposition of Claims

Claims 1-15 are currently pending in the present application. By way of this reply, claims 1 and 10 have been amended.

II. Claim Amendments

Claim 1 has been amended to recite that the gradually reducing comprises sequentially switching a plurality of devices connected to the power supply. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figures 2a and 2b of the present application.

Claim 10 has been amended to recite that the step of gradually reducing comprises a step of sequentially switching a plurality of devices connected to the power supply. No new matter has been added by way of this amendment as support for this amendment may be found, for example, in Figures 2a and 2b of the present application.

III. Rejection(s) Under 35 U.S.C § 102

Claims 1-15 of the present application were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,246,266 issued to Bosshart (hereinafter "Bosshart"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is related to techniques for reducing a magnitude of a rate of current change of an integrated circuit. With reference to the exemplary embodiment of the present invention shown in Figures 2a and 2b of the present application, a counter stage **32** is controlled to sequentially disable a plurality of transistors **34**, **36**, **38**, and **40** (via signals **C₀**, **C₁**, **C₂**, and **C₃**) so as to gradually reduce **46** an amount of current **I** sourced by a power supply **42**. Accordingly, amended independent claims 1 and 10 of the present application require, in part, gradually reducing an amount of current sourced by a power supply by *sequentially* switching a plurality of devices *connected to the power supply*.

Bosshart, in contrast to the present invention, fails at least to disclose the limitations of the claimed invention discussed above. Bosshart discloses a dynamic logic circuit, not a circuit designed to reduce a magnitude of a rate of current change. With reference to Figure 2 of Bosshart, the dynamic logic circuit **16** of Bosshart includes a precharge transistor **18_{PT}**, a precharge node **18_{PN}**, an output inverter **18_{INV}**, and a series discharge path including both a logic circuit **18_L** and a discharge transistor **18_{DT}**. See Bosshart, column 6, lines 27 – 32.

A power down mode for the dynamic logic circuit **16** is initiated by de-asserting the **ENABLE** signal. See Bosshart, column 8, lines 40 – 45. When de-asserting the **ENABLE** signal, transistors **20_{SDVN}** and **20_{SDVP}** are switched “off.” See Bosshart, column 8, line 52 – column 9, line 10. Thus, when the power down mode is entered, transistors **20_{SDVN}** and **20_{SDVP}** are switched “off” at the same time. Transistors **20_{SDVN}** and **20_{SDVP}** are *not sequentially switched* so as to reduce current sourced by the power supply as required by amended independent claims 1 and 10 of the present application. In fact, one

skilled in the art will clearly recognize that *no* plurality of devices *connected to the power supply* in the dynamic logic circuit **16** are *sequentially* switched to *reduce* current sourced by the power supply.

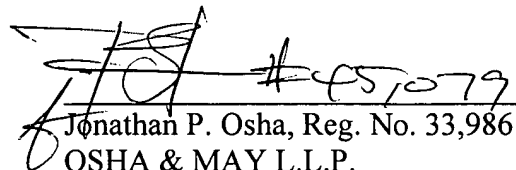
In view of the above, Bosshart fails to show or suggest the present invention as recited in amended independent claims 1 and 10 of the present application. Thus, amended independent claims 1 and 10 of the present application are patentable over Bosshart. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

IV. Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.103001; P6042).

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Respectfully submitted,


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